

WHAT IS CLAIMED IS:

Sub B6 1. A data transfer system comprising:
2 a plurality of bus devices, at least one bus device being
3 a bus data supplying device capable of supplying data, at
4 least one bus device being a bus data receiving device capable
5 of receiving data and at least one bus device being a bus
6 master device capable of requesting and controlling data
7 transfer;
8 a data bus connected to each of said plurality of bus
9 devices and capable of transferring data from a bus data
10 supplying device to a bus data receiving device under control
11 of a bus master device;
12 a direct memory access unit connected to said data bus as
13 a bus master device, said direct memory access unit including
14 a source word size register storing a source word
15 size, and
16 a target word size register storing a target word
17 size,
18 said direct memory access unit capable of transferring data
19 from a first bus data supplying device to a first bus data
20 recalling device via said first bus by recalling data from a
21 first bus data supplying device in a data size corresponding
22 to said source word data size and supplying said recalled data
23 to a first bus data receiving device in a data size
24 corresponding to said target word size.

1 2. The data transfer system of claim 1, wherein:
2 said direct memory access unit further includes

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3 a read data register loaded with data from said bus
4 data supplying device via said data bus in said source
5 word size,
6 a write data register supplying data to said bus
7 data receiving device via said data bus in said target
8 word size, and
9 a word formatter connected to transfer data from
10 said read data register to said write data register
11 thereby aligning data in said target word size in said
12 write data register.

1 3. The data transfer system of claim 2, further
2 comprising:

3 at least one first bus device being a first bus
4 supplying/receiving device capable of both supplying data to
5 said first bus and receiving data from said first bus.

1 4. The data transfer system of claim 3, wherein:

2 at least one first bus supplying/receiving device
3 consists of a central processing unit which is further capable
4 of controlling data transfer.

1 5. The data transfer system of claim 3, wherein:

2 at least one first bus supplying/receiving device
3 consists of a direct memory access unit which is further
4 capable of controlling data transfer.

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1 6. The data transfer system of claim 3, wherein:
2 at least one first bus supplying/receiving device
3 consists of a memory which is not capable of controlling data
4 transfer.

1 7. The data transfer system of claim 3, wherein:
2 at least one first bus supplying/receiving device
3 consists of a central processing unit which is further capable
4 of controlling data transfer, said central processing unit
5 connected to said direct memory access unit for loading data
6 into said source data size register and into said target data
7 size register.

1 8. The data transfer system of claim 3, wherein:
2 said direct memory access unit further includes
3 a source start address register storing a source
4 start address,
5 a source increment size register storing a source
6 increment size,
7 a target start address register storing a target
8 start address,
9 a target increment size register storing a target
10 increment size,
11 said direct memory access unit recalling data from said first
12 bus data supplying device beginning at said source start
13 address and thereafter at successive addresses differing by
14 said source increment size and supplying said recalled data to
15 said first bus data receiving device beginning at said target
16 start address and thereafter at successive addresses differing
17 by said target increment size.

Sub B6 → 1 9. The data transfer system of claim 8, wherein:
2 at least one first bus supplying/receiving device
3 consists of a central processing unit which is further capable
4 of controlling data transfer, said central processing unit
5 connected to said direct memory access unit for loading data
6 into said source start address register, said source increment
7 size register storing, said target start address register and
8 said target increment size register.

1 10. The data transfer system of claim 3, further
2 comprising:

3 a bus arbiter connected to each of said at least one bus
4 master device, said direct memory access unit and said first
5 bus, said bus arbiter granting control of data transfer on
6 said data bus to one and only one bus master device; and
7 said direct memory access unit further includes

8 a counter value register storing a number of data
9 words to be transferred by said direct memory access
10 unit,

11 a block size register storing a block size to be
12 transmitted without interruption,

13 said direct memory access unit requesting bus control from
14 said bus arbiter and upon grant of control of data
15 transmission on said data bus, said direct memory access unit
16 thereafter

17 transferring data in an amount equal to the lesser
18 of said number of data words to be transferred and said
19 block size to be transmitted without interruption,
20 thereafter

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21 ending data transfer if data transferred equals
22 said number of data words to be transmitted, and
23 suspending data transfer, releasing control of data
24 transfer on said data bus and re-requesting bus control
25 from said bus arbiter.

1 11. The data transfer system of claim 10, wherein:
2 at least one first bus supplying/receiving device
3 consists of a central processing unit which is further capable
4 of controlling data transfer, said central processing unit
5 connected to said direct memory access unit for loading data
6 into said counter value register and said block size register.

1 12. The data transfer system of claim 1, wherein said
2 plurality of bus devices consist of first bus devices and said
3 data bus consists of a first data bus, said data transfer
4 system further comprising:

5 a plurality of second bus devices, at least one second
6 bus device being a second bus data supplying device capable of
7 supplying data, at least one second bus device being a second
8 bus data receiving device capable of receiving data and at
9 least one second bus device being a second bus master device
10 capable of requesting and controlling data transfer, each
11 second bus device having a predetermined data size;

12 a second data bus having said predetermined data size
13 connected to each of said plurality of second bus devices and
14 capable of transferring data from a second bus data supplying
15 device to a second bus data receiving device under control of
16 a second bus master device;

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21 wherein said direct memory access unit stores said
22 predetermined data size in said source word size register for
23 data transfer from a second bus device to a first bus device
24 via said bus bridge and stores said predetermined data size in
25 said target word size register for data transfer from a first
26 bus device to a second bus device via said bus bridge.